Revolutionary Advances in Distributed Power Systems

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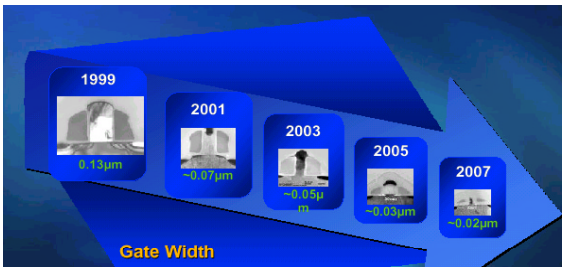
Abstract – Rising power demands and increasing number of supply voltages required in modern communications and computing systems are driving advancements in distributed power architectures. Primary-side isolated 48V power modules have matured with Single and Dual-outputs (+3.3V & +5V) achieving ultra-high density and greater efficiency. Secondary-side PWM controllers have evolved to higher frequency and efficiencies and are giving way to yet another distributed power concept, the quasi-regulated +12V single-output power module. Several power module manufacturers are now offering this new +12V Brick driven by demands from the system OEMs. In this paper we explore ever changing distributed power architectures, integrated PWM circuitry and new distributed power supply topologies that are enabling new information infrastructure systems.

I. Introduction

Today's power supply design challenge is one of creating multiple-output DC/DC converters with tight regulation on multiple low-voltage outputs connected to high slew rate dynamic loads. New generations of power supply architectures and specialized PWM controllers are emerging to meet these demands [1]. Two application areas having quite separate challenges in the past are beginning to converge; the 12V desktop power supply and the –48V telecom power supply. Both of these applications present unique challenges that are shaping the future of the power topologies and the power control technology used in modern DC/DC converters.

II. High-Performance Systems

At the heart of communication systems and Desktop PCs are advanced microprocessors and high-speed communication ASICs designed in deep sub-micron, low-voltage CMOS logic technologies (Figure 1.). Operating at GHz clock frequencies and supplying large currents (over 60A) on multiple tightly regulated, low-voltage supply rails (sub-2Vdc), presents major challenges to the DC/DC power conversion system. In order to protect the expensive system chips from potentially destructive power conditions, multiple supply rails must be sequenced on-and-off in a prescribed order and ramped up and down within a finite amount of time and minimal overshoot beyond the desired output level.



Lower Voltage, Higher Current Loads

- **Finer and finer Gate Widths**
- **Dramatic increases in power and bandwidth**
- **Trillions of instructions per second**

Source: Intel IDF 9/02

Figure 1. Advanced CMOS leading way to sub 1V supply

III. New Power Topologies

New power supply topologies are emerging to meet the power conversion challenges of these modern computing and communication systems. In communication systems traditional –48V isolated power supply topologies (single-ended forward and flyback regulators) are yielding the way to higher power topologies (Push-pull, and Half-bridge & Full-bridge). Also new hybrid topologies, such as cascaded regulators are emerging. In computer systems, traditional non-isolated PC power supply topologies (multiphase buck regulators) are yielding the way to isolated power conversion topologies that take advantage of the transformer turns-ratio to create multiple low-voltage outputs in one conversion step to provide the many low voltage rails required by advanced microprocessors.

These ever changing power supply considerations create fresh opportunities for PWM control IC designers to match new process technologies with unique power integrated circuit design techniques to develop the next generation power system requirements.

IV. Reversing Roles in Distributed Power

A reversal in the roles of the traditional distributed power conversion architectures is emerging between computer and communication systems. Desktop PC power architectures are being proposed that develop multiple low voltage supply rails from a +48V bus rather than a +12V distributed bus. This allows reduces the distribution losses expected with the ever-increasing power appetite of next generation processors. Conversely, telecom power architects are just now launching a new DC/DC modules to convert the – 48V bus to a +12V distributed bus so they can take advantage of the vast array of point of load power controllers available on the market today (Figure 2.).

Some high-end workstation and server systems already use a +48V distributed power conversion system that maintains proper regulation while supplying very high load currents. Due to the difficulty in achieving tight regulation on supplies with ever decreasing load voltages and geometrically increasing load currents, a +48V distributed power system is now being considered to replace the traditional +12V bus in desktop PC power supplies [2].

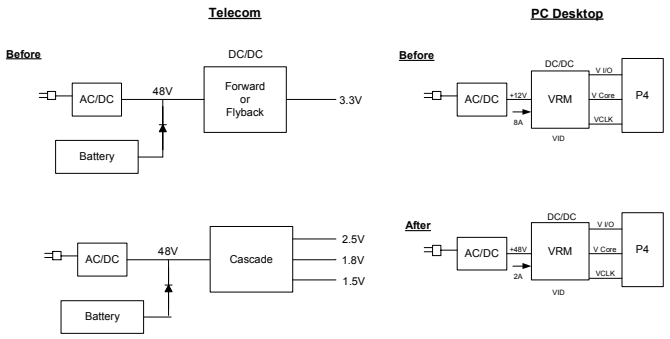


Figure 2. Reversing Roles in Distributed Power Architectures

V. Segmenting Centralized and Distributed Power

A. Centralized Power

The term "centralized power" originated in early 1980's when a typical AC/DC power supply came package in a silver-box chassis with an AC line cord on one side and a DC cable harness out the other side of the chassis for mating with a system power connector. Multiple DC voltages (typically +12V, +/-5V, +3.3V) where provided through the connector to the PCB power planes. Advanced sub-micron CMOS technology emerged in the early 90's changing the power supply requirements from traditional +5Vdc and +3.3V supplies to multiple non-standard low voltage supplies (2.5V, 1.8V, 1.2V, etc.) with high load currents being demanded by advanced microprocessors and ASICs.

B. Distributed Power

A combination of high slew-rate load currents and tight regulation specifications for very low-voltage outputs gave rise to usage of "distributed power" with point of load converters. In a distributed power system a single intermediate voltage (typically +12V or +48V) is generated by an offline AC/DC supply and converted to lower voltages with a DC/DC regulator located on the motherboard closer to the point of the loading (Fig 2). The close proximity of the DC/DC regulator to the high slew-rate load reduces distribution impedances permitting more precise and easier to control regulation. Reduced parasitic elements in the control loop, lower voltage drop across the PCB power planes and a cost savings for distribution cables and connectors.

C. Hybrid "Centralized-Distributed" Power

Modern desktop PCs use a hybrid "Centralized-Distributed" power system. They deploy a classical centralized multi-output AC/DC power supply (silver-box), and distribute a +12V output through a power plane to a DC/DC converter (called Voltage-Regulation-Module – VRM) that is located near the microprocessor. These strategically placed VRM converters are able to provide precision low voltage and high current power supply outputs demanded by advanced microprocessors with minimal interference from parasitic elements of the power distribution system.

D. - 48Vdc Distributed Power

Distributed Power systems were first used in telecommunication (base stations and central offices) and data communication applications (switches, routers, hubs). A back-up battery voltage of - 48V is distributed throughout a back plane of a rack mounted system that houses several plug-in boards and line cards. Each card may use one or more DC/DC converters (board mounted power modules called Bricks) to first isolate and then convert the – 48V input to a lower voltage closer to the point-of-loading (Figure 3.). These power modules are available from many suppliers in a standardized footprint, with single or multiple output voltages and at various power levels (30W up to 1000W).

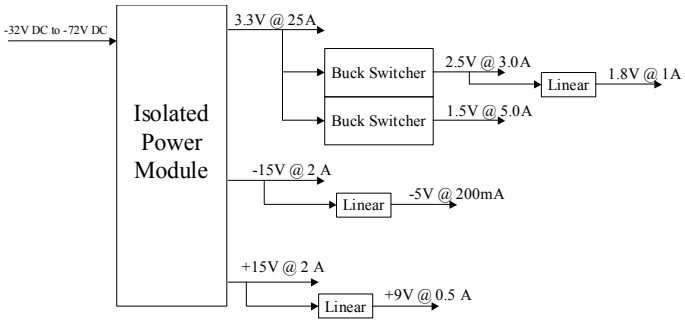


Figure 3. Communication System –48V Distributed Power

1) 48V Telecom Power Module "Bricks"

a) Full & half-Bricks

Volume 2.1 to 4.2 inch^3
Density: 100 W to 150W per inch^3
Greater than 90% efficiency
48V Nom. Vin (2:1 range; 36V to 72V)
1% Regulation Tolerance
(@ 1.8Vout; 100mV drop is 6% tolerance)

b) Sub-Bricks

(Volume 0.65 to 1.5 inch^3)

Quarter-Brick Modules:
100W+ (depending on airflow)

Eighth-brick format
50% -65% smaller than ¼ brick
50W+ (depending on airflow)

Figure 4. –48V Telecom Power Modules (Bricks)

2) Feedback Issues:

a) Galvanic safety isolation – 500VRMS.
b) Noise immunity – prevent ground-shifts in common grounded systems.
c) Opto-couplers – thermal performance, aging, reliability, bandwidth issues.
d) Magnetic Feedback techniques – open-loop, galvanic isolated, noise filtering.

3) Planar Magnetic Transformers

Deploy Copper traces in the multiplayer PCB board to form windings of the transformer (Figure 5.). Automatic production and interconnection avoids the added costs associated with labor-intensive builds of traditional wire wound transformers. Consistent and repeatable parasitic leakage inductance and distributed capacitances can be guaranteed with planar transformers that lower the risk and cost of test failures.

Figure 5. Planar Magnetic Transformers

VI. Next Generation DC/DC Converters

To meet the challenge of creating multiple low-voltage outputs off a single 48V distributed power supply rail, new two-stage architectures and their associated integrated PWM controllers have been successfully deployed [3][4]. These power supplies "cascade" two converter stages in series, such as a Buck-Fed Push-Pull, Buck-Fed Half-Bridge, or a Push-Pull-Fed Bank-of-Bucks (Figure 6).

A. Cascaded "Buck-Fed" Topology

The Cascaded "Buck-Fed" topology is used to efficiently generate multiple low voltage outputs using a low-cost transformer-isolated power conversion technique. A traditional non-isolated Buck regulator first chops the 48V

input (approximately in half), which powers an isolated second stage (such as a Push-pull or half-bridge). The isolation transformer turns-ratio completes the step-down conversion to single or multiple low-voltage DC outputs. These output voltages are regulated by PWM control of the Buck stage while the push-pull stage operates at constant duty cycle for continuous power transfer to the output(s).

B. Cascaded "Buck-Follower" Topology

The Cascaded "Buck-Follower" topology is emerging as an attractive alternative when multiple tightly regulated outputs are required. The first stage of a Cascaded Buck-Follower delivers a single +12V output from a low-cost transformer isolated power converter (push-pull or half-bridge), which powers any number of point of load Buck regulators. This two-stage architecture uses an open-loop transformer isolated chopper to provide the quasi-regulated 12V (7V – 13V) secondary voltage that is distributed across the system motherboard and converted to the required output voltages at the point-of-loading.

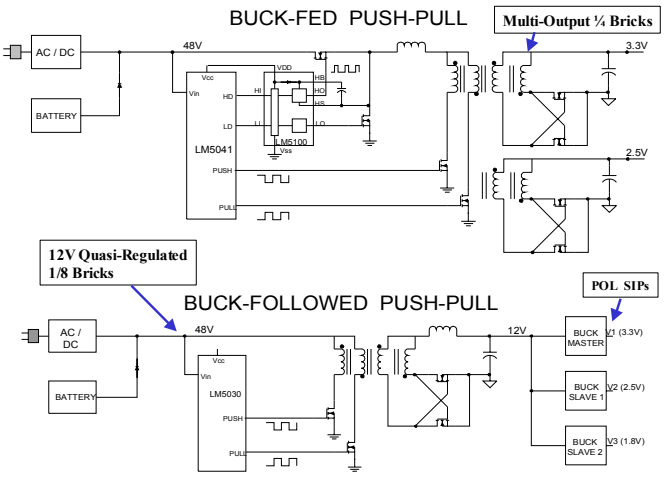


Figure 6. Buck-Fed and Buck-Followed Topologies

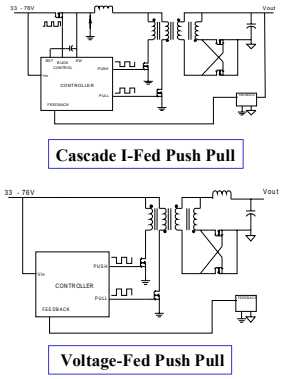
VII. Design of Multi-Output Power Supplies

Traditional multi-output power supplies use a single isolation power transformer to generate multiple secondary voltages. They provide galvanic isolation using a high frequency transformer with multiple secondary windings. These multi-output converters feedback and regulate a single, most critical output and the other "slaved" outputs are cross-regulated with less accuracy since they are not directly controlled by the PWM regulation loop. Traditionally, isolated power supplies use the flyback or forward topologies, which are lower cost to build but have limited efficiency and poor regulation across multiple outputs.

A newer topology, called the Cascaded "Buck-Fed" Push-Pull (or half-bridge) converter provides for tighter voltage regulation (Figure 7.). Unlike a forward converter, the cascaded converter offers outstanding cross-regulation properties with reduced cost and complexity by eliminating output filter inductors and current sense resistors. In the current-fed push-pull converter, the output circuit resembles a flyback regulator, without a filter inductor. No output voltage regulation error is induced from the inductor parasitic connection resistances. Also, the push-pull transformer is continuously driven at exactly 50 % duty-cycle to produce a continuous power flow to the outputs. This optimizes the isolation transformer core utilization, reduces output component stresses, and reduces noise, which makes this topology well suited for high output power applications. The cascaded topology also offers excellent cross-regulation during a load transient event since the filter capacitors on the multiple outputs act as if they were in parallel to supply the needed transient power.

A. Current-Fed Push-Pull Converter Advantages:

1) Good for high power multi-output converters
2) Primary-side Buck inductor serves as filter for multiple outputs
3) Low secondary side parasitic components (Winding & SyncFET Resistance)
4) Push-pull provides Continuous output power for improved transient response
5) Reduced voltage stresses on primary Push-Pull and secondary-side SyncFETs
6) Coupled transformer inductance improves cross regulation characteristic
7) Overlap control tunes out ripple voltage noise from outputs



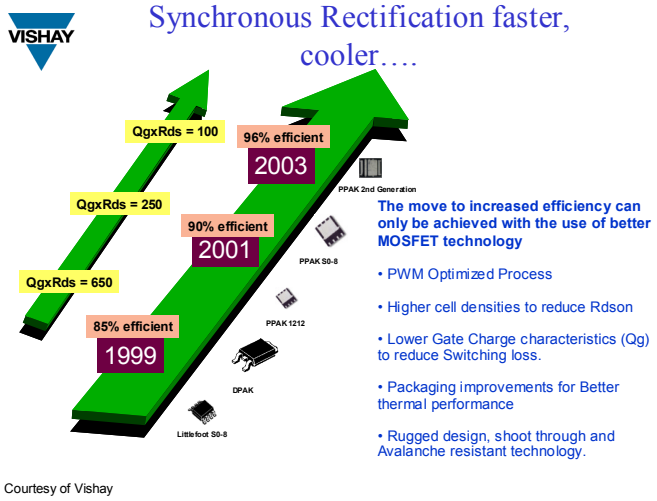
Current Fed Advantages

A few More Part, but ;

- *Lower Losses*
- *1%-3% efficiency advantage*

Parameter	Current Fed	Voltage Fed
MOSFETS	5	4
P-P SW Duty Cycle	100%	50%
SW Current	1X	2X
Losses (Estimated)	7.5%	8.5%
CFPP Buck	3.0%	
Pri SW Current	1.0%	2.0%
Pri Switching	1.5%	2.5%
Output SW Current	1.5%	3.0%
Output Cross Conduction	0.5%	1.0%
INDUCTOR		
Inductor Current	1X	4X
Inductance	16X	1X
LI^2 product	4	16
Resistance	2X	1X
Resistive Loss	2	16

Figure 7. Current-Fed versus Voltage-Fed Push-Pull



Courtesy of Vishay

Figure 8. Modern Power Semiconductor Technology

VIII. Modern Power Semiconductor Technologies

Advances in controller circuitry and thermal design make it possible to pack significant power conversion systems into smaller and smaller spaces. Advances in Power MOSFET technology have led to significant reductions in power dissipation leading to increased power conversion efficiency. New power semiconductors have reduced RDSon and gate threshold voltage to reduce the conducted and switching losses while controlling the parasitic gate capacitance to allow faster switching speeds (Figure 8.). These power MOSFETs are also deployed in the secondary-side of the converter as Synchronous Rectifiers to aid in reducing rectifier losses. The combination of advancements in power architectures, high-voltage Cascaded PWM controllers and power MOSFET are allowing power supply designers to develop smaller and more efficient DC/DC converters that are capable of producing multiple-low-voltage and high current outputs required by dense, deep-sub-micron microprocessors and ASICs used in modern computing and communication systems.

IX. Modern PWM Controller Design Challenges

New cascade PWM controllers must overcome the challenges of integrating two PWM controllers in ever decreasing package sizes. A high-voltage (100V) IC technology is required for the controller to operate directly off the 48V input line and survive a 100V transient voltage spike. Tiny, thermally enhanced packages dissipate the thermal load in a smaller PC board footprint, while reducing junction temperature for improved reliability. A perfect balance of high-voltage technology, thermally enhanced package technology, and innovative circuit design techniques are the heart of the new Cascaded Buck-Fed PWM Controllers (Figure 9).

Features
- Internal Start-up Bias Regulator
- Programmable Line Under Voltage Lockout (UVLO) with Adjustable Hysteresis
- Current Mode Control
- Internal Error Amplifier with Reference
- Dual Mode Over-Current Protection
- Programmable Push-Pull Overlap or Deadtime
- Internal Push-Pull Gate Drivers
- Programmable Soft-Start
- Programmable Oscillator with Sync Capability
- Precision Reference
- Thermal Shutdown (165°C)

Packages: TSSOP16 and LLP16 (5 x 5 mm)

Typical Applications
- Telecommunication Power Converters
- Industrial Power Converters
- Multi-Output Converters
- +42V Automotive Systems

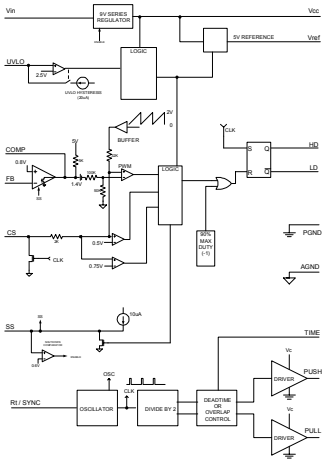


Figure 9. LM5041 (100V) Cascaded PWM Controller

X. Evolutions in High-voltage PWM Technology

National Semiconductor has developed a new family of high voltage ABCD (Analog Bipolar-CMOS-DMOS) technologies with sufficient breakdown voltages for 48V power systems. The high voltage technologies are based on the ABCD150 platform that supports highly integrated power management products (Simple Switchers) operating at 50V and below.

Two new technologies, ABCDXV1 and ABCDXV2, enhance the breakdown voltages of the n-channel DMOS power transistors, high voltage PMOS and junction isolation diode to withstand worst-case 100V+ transients (Figure 10.). Increasing the Epitaxy thickness and selectively modifying Epitaxy doping of the original ABCD150 process achieved the increased breakdown voltages. TCAD simulation of the DMOS array termination and metal field plate yielded the desired breakdown performance with relatively minor changes in the Epitaxial process parameters. The use of an additional N-Well implant in the DMOS drain region moderates the increase in DMOS on resistance normally associated with higher voltage Epitaxy. The N-Well doping also maintains the minimum gate length and punch-through voltages of the PMOS logic devices fabricated in the Epitaxy.

ABCD150HV / XV1 Specifications

Technology Type	Analog BiCMOS/DMOS
Interconnect	Dual Metal
Max Operating Voltage	80 V VDMOS, 10 V NMOS & PMOS -40 V Lat PNP, 15 - 20V NPN
Epi Substrate BV	80V (HV) and 100V (XV1)
Min. Feature Size	1.5 µm
Minimum Metal Pitch	3.5 µm
No. Of Masks	20
Wafer Diameter	6"
Fab Site	UK
Device Structures	NPN, Lateral PNP VDMOS, Lateral DMOS, LV NMOS, PMOS and Drain Extention for HV NMOS & HV DMOS, P-Body Resistors

Figure 10. High-voltage BCD Technology

XI. Design Features in new PWM Controllers

A. High-voltage Start-up regulator

The function of this high voltage circuit is to provide bias power to the controller upon initial start-up. Providing this function with the main power controller allows the line voltage to be connected directly the controller. Following initial power-up, an auxiliary winding from the main transformer or output inductor most often provides the bias power. The start-up regulator should be current limited and have thermal shutdown protections.

B. Line Under Voltage Lockout (UVLO)

This feature is necessary to shut the converter off at low line conditions. The power converter input can be viewed as a constant power load. As the line voltage decreases the input current increases. At some point the input current can rise to dangerous levels. Once any comparator function such as line under voltage lockout is added, hysteresis will become necessary. How much hysteresis is required will depend upon the source impedance, input filter impedance, softstart timing and output loading. It is therefore desirable to have adjustable UVLO hysteresis.

C. High Voltage Level Shifted Gate Drivers

Buck and Bridge topologies present a problem of driving the gate of the high side switch(es). New high-voltage processes can now incorporate level shift for on chip floating Buck gate drivers.

D. Thermal Shutdown

Controllers are getting forced into smaller and smaller packages, while the feature sets are forever increasing. Abnormal operating conditions can quickly raise the operating junction to potentially damaging levels. A chip thermal shutdown circuit can prevent catastrophic damage.

E. User programmable Dead-time and Overlap-time

Critical timing relationships exist amongst the switch driver outputs of high-performance controllers. Synchronous Buck regulators require a small dead time between turn-on and turn-off of the switches to avoid a catastrophic shoot-through condition. Too much dead-time leads to excessive body diode conduction and increased power loss. In the Cascaded Buck-Fed Push-Pull Converter, an overlap time is

desired in the Push-Pull power transistors to maintain a current path critical for continuous conduction of the Buck inductor. Failure to maintain a conduction path can lead to catastrophic avalanche breakdown of the Push-pull Power transistors. Controllers which have the ability to either predict or adapt the timing gives designers the most flexibility to optimize the converter.

F. Multiple Controllers in a Single Package

High density multiple output power bricks are becoming very popular. This approach has both a cost and volume savings at the system level. Controllers to drive Cascaded converters having two pulse width modulators on a single chip save cost and board space.

X. Conclusions

This paper presents the evolving distributed power architecture and associated PWM control technologies used in modern telecommunication and computing systems. New power module topologies and PWM controllers that have emerged to aid power supply architects in the design of low profile, ultra-efficient power modules. Application issues are eased using the latest distributed power architectures including safety and noise, how to drive synchronous rectifiers, ease of control schemes, and component cost required to increase efficiency.

Two new emerging cascaded converter topology's, the Buck-follower and Buck-Fed converters and new controller features are presented with important tradeoffs that assists power architects in determining which new topologies are best suited for their applications.

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